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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL W. MORROW

Appeal 2007-3972
Application 10/027,978[1]
Technology Center 2100

Decided: May 8, 2008

Before JAMES D. THOMAS, JEAN R. HOMERE, and
CAROLYN D. THOMAS, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 14 through 28. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

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[1] Filed on Oct. 24, 2001. The real party in interest is Intel Corp.

The Invention

Appellant invented a computer apparatus for reducing latency in a virtual-to-physical address translation process by moving a table walk logic as closely as possible to a virtual memory. As depicted in Figure 1, the apparatus (110) includes a table walk device (170) coupled to a memory controller (160), which interfaces with a virtual memory (190) and a memory management unit (150) coupled to a translation look-aside buffer (140). The table walk device (170) retrieves address information from translation tables stored in virtual memory (190) to perform the virtual to physical address translation. (Spec. 4-9.)

An understanding of the invention can be derived from exemplary independent claims 14 and 23, which read as follows:

14. An apparatus, comprising:

a memory controller; and

a table walk device connected to the memory controller and externally located from a memory management unit (MMU).

23. A system, comprising:

a processor;

a discrete memory controller adapted to perform a table walk operation and coupled to the processor; and

a volatile memory device coupled to the discrete memory controller.

In rejecting the claims on appeal, the Examiner relied upon the following prior art:

Zolnowsky	US 4,766,537	Aug. 23, 1988
McCarthy	US 5,666,509	Sep. 09, 1997
Roth	US 5,937,437	Aug. 10, 1999
Arimilli	US 6,658,538 B2	Dec. 02, 2003 (filed Jun. 21, 2001)
Gaskins	US 6,681,311 B2	Jan. 20, 2004 (filed Jul. 18, 2001)

The Examiner rejected the claims on appeal as follows:

1. Claims 23, 24, and 26 through 28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gaskins.

2. Claims 14, 17, and 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli.

3. Claims 14 through 18, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McCarthy and Roth.

4. Claims 19, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of McCarthy, Roth, and Zolnowsky.

5. Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Gaskins and McCarthy.

6. Claims 15, 16, and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Arimilli and McCarthy.

7. Claims 19, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Arimilli and Zolnowsky.

FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Gaskins

1. As depicted in Figure 1, Gaskins discloses a data unit (100) of a microprocessor that includes a table walk logic (106) coupled to a translation lookaside buffer (TLB-102) that caches a plurality of virtual addresses to be translated into physical addresses. (Col. 4, ll. 1-9, ll. 60-63.)

2. Gaskins discloses that, upon receiving a miss signal from the TLB (102), the table walk logic (106) performs a page table walk to obtain a page table entry (PTE) associated with a virtual address, and outputs the PTE (152) to the TLB (102) for caching. (Col. 6, ll. 4-10.)

3. Gaskins discloses that the data unit (100) also includes a processor bus (148) that interfaces the microprocessor with other devices within the computer system such as memory controllers, I/O devices and with other microprocessors. (Col. 4, l.60- col. 5, l. 5.)

Arimilli

4. As shown in Figure 2, Arimilli discloses a central processing unit (CPU-20) that includes a table walk controller (78) externally coupled to a data memory management unit (DMMU-48) and an instruction memory management unit (IMMU-50) to translate addresses of data and instructions, respectively into virtual addresses and then into physical addresses supplied to data caches (42, 44, 46.) (Col. 8, ll. 1-7.)

5. The table walk device (78) is also connected with a memory controller (MC-24) that controls access to an associated one of the physical system memories. (Col. 4, ll. 35-38.)

McCarthy

6. As depicted in Figure 2, McCarthy discloses a data cache unit (16) having a memory controller (26) coupled to a memory management unit (MMU-32). As shown in Figure 3, the MMU (32), in turn, includes a controller (44) coupled to a table walk controller (42). (Col. 4, ll. 10-15, ll. 38-54.)

Roth

7. As depicted in Figure 1, Roth discloses a processor (100) having an IMMU (124) and a DMMU (134), each having with a TLB (128, 138, respectively) to translate virtual addresses to physical addresses. (Col. 3, ll. 27-59.)

PRINCIPLES OF LAW

ANTICIPATION

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the

claim at issue "reads on" a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

OBVIOUSNESS

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

> "Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007).

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might

be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results."). *Leapfrog Enter., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (quoting *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41(2007)). "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims." *KSR*, 127 S. Ct. at 1742.

Discussing the obviousness of claimed combinations of elements of prior art, *KSR* explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.*, 425 U.S. 273 (1976)] and *Anderson's-Black Rock*[*, Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740. Where the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a

showing that there was "an apparent reason to combine the known elements in the fashion claimed." *KSR*, 127 S. Ct. at 1741. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, 127 S. Ct. at 1741 (quoting *In re Kahn*, 441 F.3d 977, 987(Fed. Cir. 2006)).

The reasoning given as support for the conclusion of obviousness can be based on interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art. *KSR*, 127 S. Ct. at 1740-41. *See also Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2007).

We note our reviewing court has recently reaffirmed that:

> [A]n implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the 'improvement' is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient. Because the desire to enhance commercial opportunities by improving a product or process is universal—and even common-sensical—we have held that there exists in these situations a motivation to combine prior art references even absent any hint of suggestion in the references themselves. In such situations, the proper question is whether the ordinary artisan possesses knowledge and skills rendering him capable of combining the prior art references.

Leapfrog, 485 F.3d at 1162 (holding it "obvious to combine the Bevan device with the SSR to update it using modern electronic components in order to gain the commonly understood benefits of such adaptation, such as

decreased size, increased reliability, simplified operation, and reduced cost").

Also, a reference may suggest a solution to a problem it was not designed to solve and thus does not discuss. *KSR*, 127 S. Ct. at 1742 ("Common sense teaches . . . that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. . . . A person of ordinary skill is also a person of ordinary creativity, not an automaton.").

The prior art relied on to prove obviousness must be analogous art. As explained in *Kahn*,

> the 'analogous-art' test . . . has long been part of the primary Graham analysis articulated by the Supreme Court. *See Dann* [*v. Johnston*,] 425 U.S. [219,] 227-29 (1976), *Graham*, 383 U.S. at 35. The analogous-art test requires that the Board show that a reference is either in the field of the applicant's endeavor or is reasonably pertinent to the problem with which the inventor was concerned in order to rely on that reference as a basis for rejection. *In re Oetiker*, at 1447. References are selected as being reasonably pertinent to the problem based on the judgment of a person having ordinary skill in the art. *Id.* ("[I]t is necessary to consider 'the reality of the circumstances,'—in other words, common sense—in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor." (quoting *In re Wood*, 599 F.2d 1032 (C.C.P.A. 1979))).

Kahn, 441 F.3d at 986-87. *See also In re Clay*, 966 F.2d 656, 659 (Fed. Cir. 1992) ("[a] reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because

of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem.").

In view of KSR's holding that "*any* need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed," 127 S. Ct. at 1742 (emphasis added), it is clear that the second part of the analogous-art test as stated in *Clay*, *supra*, must be expanded to require a determination of whether the reference, even though it may be in a different field from that of the inventor's endeavor, is one which, because of the matter with which it deals, logically would have commended itself to an artisan's (not necessarily the inventor's) attention in considering *any* need or problem known in the field of endeavor. Furthermore, although under *KSR* it is not always necessary to identify a known need or problem as a motivation for modifying or combining the prior art, it is nevertheless always necessary that the prior art relied on to prove obviousness be analogous. *See KSR*, 127 S. Ct. at 1739. ("The Court [in *United States v. Adams,* 383 U.S. 39, 40 (1966)] recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another *known in the field*, the combination must do more than yield a predictable result.") (emphasis added). *See also Sakraida*, 425 U.S. at 280

> ("Our independent examination of that evidence persuades us of its sufficiency to support the District Court's finding 'as a fact that each and all of the component parts of this patent . . . were old and well-known throughout the dairy industry long prior to the date of the filing of the application for the Gribble patent.'").

ANALYSIS

102 Rejections

Claims 23-24 and 26-28

Independent claim 23 recites in relevant part a discrete memory controller adapted to perform a table walk operation and coupled to a processor. (App. Br., Appendix A.) Appellant argues that Gaskins does not teach that limitation. Particularly, Appellant submits that even though Gaskins' table walk logic can perform table walk operations, it is not a discrete memory controller coupled to a processor unit since the table walk logic is part of a processor itself. (App. Br. 7.) The Examiner, in response, avers that Gaskins' table walk logic does teach the discrete memory controller since, similarly to the Appellant's controller, it performs the claimed table walk operations, which are memory controlling functions. (Ans. 11-12.)

Therefore, the pivotal issue before us is whether one of ordinary skill in the art would find that the table walk logic disclosed in Gaskins' data unit teaches a discrete memory controller, as claimed. We answer this inquiry in the affirmative.

We begin by considering the scope and meaning of "discrete memory controller," which must be given its broadest reasonable interpretation consistent with Appellant's disclosure, as explained in *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997):

> [T]he PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of

> definitions or otherwise that may be afforded by the written description contained in the applicant's specification.

Id. at 1054. *See also In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989) (stating that "claims must be interpreted as broadly as their terms reasonably allow." Appellant's Specification states the following:

> Memory controller 160 may be adapted to control memory 190.

(Spec. 7, l. 4.)

> [M]emory controller (160) may be adapted to perform a virtual-to-physical address translation by, for example, integrating table walk device 170 with memory controller 160.

(Spec. 11, ll. 1-4.)

Our reviewing court further states, "the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005).

Upon reviewing Appellant's Specification, we fail to find any definition of the term "discrete memory controller" that is different from the ordinary meaning. We find the ordinary meaning of the term "controller" is best found in the dictionary.[2] Therefore, we interpret a "discrete memory controller" as a device that manages logical and physical accesses to a memory device.

As detailed in the findings of facts section above, Gaskins discloses that the table logic performs translation of virtual addresses to physical addresses when a TLB coupled thereto indicates that a miss has occurred during a translation. (FF. 1-2.) Further, Gaskins discloses that the table

[2] A controller is a device upon which other devices rely for access to a computer subsystem. It controls access to one or more disk drives, managing physical and logical access to the drive or drives. (Microsoft Press Computer Dictionary, Second Edition, 1993, p. 95.)

walk logic accesses the TLB to retrieve addresses to be translated, and subsequently returns the translated addresses to the TLB. (*Id.*) Additionally, Gaskins discloses that the data unit may be connected to another microprocessor via a processor bus. (FF. 3.) One of ordinary skill in the art would readily recognize that Gaskin's table walk logic, by accessing the TLB memory to retrieve addresses and by returning the translated addresses to the TLB for subsequent storage, manages data in the TLB. Therefore, under our interpretation above, Gaskins' table walk logic teaches the discrete memory controller. Further, the ordinarily skilled artisan would also recognize that Gaskins' memory controller is adapted to perform a table walk operation when the TLB reports that a miss has occurred during an address translation. Additionally, the ordinarily skilled artisan would recognize that the table walk logic is coupled to a microprocessor since the data unit, which houses the table walk logic can be connected to another microprocessor via a host bus.

Appellant further argues that the Gaskins reference "teaches away" from the invention as claimed (App. Br. 7.) We find Appellant's "teaching away" argument is misplaced, because the Examiner has rejected the claims under 35 U.S.C. § 102. Our reviewing court has determined that "[t]eaching away is irrelevant to anticipation." *Seachange International, Inc., v. C-Cor, Inc.*, 413 F.3d 1361, 1380 (Fed. Cir. 2005).

It follows that Appellant has not shown that the Examiner erred in finding that Gaskins anticipates independent claim 23.

Appellant does not provide separate arguments with respect to the rejection of claims 24, and 26 through 28. Therefore, we select claim 23 as

being representative of the cited claims. Consequently, claims 24, and 26 through 28 fall together with representative claim 23. 37 C.F.R. § 41.37(c)(1)(vii).

Claims 14, 17, and 20

Independent claim 14, recites in relevant part a table walk device connected to a memory controller and externally located from a memory management unit. (App. Br., Appendix A.) Appellant argues that Arimilli does not teach that limitation. (App. Br. 8.) Particularly, Appellant argues that even though Arimilli teaches a memory controller coupled to a table walk device, and externally coupled two MMUs in a single CPU, the MMUs are not in direct physical connection with the memory controller. (App. Br. 8.) In response, the Examiner submits that Arimilli's CPU discloses the claimed connection between the table walk device, the MMUs and the memory controller. (Ans. 14.) We agree with the Examiner.

As detailed in the Findings of Fact above, Arimilli discloses a CPU that includes a table walk controller externally coupled to two MMUs. (FF. 4.) As acknowledged by Appellant, Arimilli further discloses that the table walk controller communicates with a memory controller. (FF. 5, App. Br. 8.) Therefore, the ordinarily skilled artisan would aptly recognize that the memory controller is connected to the table walk device. Similarly, the ordinarily skilled artisan would recognize that the table walk device is externally coupled to the MMUs. Further, we note that Appellant's claim do not require the memory controller to be in direct physical connection with the table walk device. Therefore, Appellant's argument that Arimilli does

not teach such direct physical connection has no basis here in this appeal. Similarly, Appellant's argument that Arimilli teaches away from the invention is misplaced. *See Seachange International.* It follows that Appellant has not shown that the Examiner erred in finding that Arimilli anticipates claim 14.

Appellant does not provide separate arguments with respect to the rejection of claims 17 and 20. Therefore, we select claim 14 as being representative of the cited claims. Consequently, claims 17 and 20 fall together with representative claim 14. 37 C.F.R. § 41.37(c)(1)(vii).

103 Rejections

Claims 14-18, 20

Appellant argues that the combination of McCarthy and Roth does not teach a table walk device externally located from the memory management unit (MMU), as recited in claim 14. (App. Br. 10-11.) We agree with Appellant.

As set forth in the Findings of Facts section, McCarthy discloses an MMU including a table walk device connected to a memory controller. (FF. 6.) Further, Roth discloses a processor having two MMUs, each including a TLB to translate virtual addresses to physical addresses. (FF. 7.) One of ordinary skill would have readily recognized that the combination of McCarthy and Roth teaches, at best, an MMU including a table walk device connected to a memory controller. However, the ordinarily skilled artisan would have recognized that the disclosed table walk device is internally located in the MMU. Thus, the disclosed table walk device is not externally

located from the MMU, as claim 14 requires. It follows that Appellant has shown that the Examiner erred in concluding that the combination of McCarthy and Roth renders claim 14 unpatentable.

Claims 15 through 18, and 20 incorporate the limitations of independent claim 14 by dependency. Consequently, for the reasons detailed in the discussion of claim 14 above, Appellant has shown that the Examiner erred in concluding that the combination of McCarthy and Roth renders claims 15 through 18 and 20 unpatentable.

Claims 19, 21, and 22

Appellant argues that Zolnowsky does not cure the deficiencies of the McCarthy-Roth combination. (App. Br. 12.) We agree.

As noted in our discussion of independent claim 14 above, the McCarthy-Roth combination fails to teach an MMU externally located from a table walk device. The Examiner's reliance on Zolnowsky is not concerned with remedying this deficiency. Therefore, Appellant has shown that the Examiner erred in concluding that the combination of McCarthy, Roth, and Zolnowsky renders claims 19, 21, and 22 unpatentable.

Claim 25

Appellant argues that the combination of Gaskins and McCarthy does not render dependent claim 25 unpatentable since McCarthy does not cure the deficiencies of Gaskins with regard to independent claim 23 from which claim 25 depends. (App. Br. 13.) This argument is unavailing. In our

discussion of independent claim 23 above, we found no such deficiency in the Gaskins reference for McCarthy to cure.

Next, Appellant merely recites the language of claim 25 and alleges that the recited limitations are not found in the combination of Gaskins and McCarthy. (Id.) In response, the Examiner asserts that McCarthy discloses an MMU including an ATC adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device. (Ans. 8, 20-21.) We note that Appellant has failed to particularly address the Examiner's specific findings of fact as set forth in the rejection. (*Id.*) Appellant's gratuitous allegations without providing a scintilla of evidence are insufficient to overcome the Examiner's prima facie case of obviousness.

Last, Appellant argues that there is insufficient rationale to support the proffered combination of Gaskins and McCarthy. (App. Br. 13-14.) As detailed in our discussion of claim 23 above, Gaskins teaches a discrete memory controller adapted to perform a table walk operation, and coupled to a processor. Further, as discussed above, McCarthy discloses an MMU including a memory controller connected to table walk device, as well as an ATC adapted to provide memory access protection. Therefore, McCarthy's use of the MMU would have suggested to the ordinarily skilled artisan to protect access to a memory device such as Gaskins' to *predictably result* in a computer system having an MMU to protect access to a memory device. Therefore, Appellant's allegation that there is insufficient rationale to combine the cited references is not persuasive. The Supreme Court has held that in analyzing the obviousness of combining elements, a court need not

find specific teachings, but rather may consider "the background knowledge possessed by a person having ordinary skill in the art" and "the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l*, at 1740-41. To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 1740. As set forth in the preceding paragraph, using an MMU to protect access to a memory device in a computer system is prior art teaching that is being used in a conventional memory management system for the known purpose of fending off unauthorized users.

It follows that Appellant has not shown that the Examiner erred in concluding that the combination of Gaskins and McCarthy renders claim 25 unpatentable.

Claims 15, 16, and 18

Appellant argues that McCarthy does not cure the deficiencies of Arimilli as it pertains to the rejection of claim 14 from which claims 15, 16, and 18 depend. (App. Br. 14-15.) As detailed in our discussion of claim 14, we found no such deficiencies in Arimilli for McCarthy to cure. Further, Appellant argues that McCarthy teaches away from Arimilli. (*Id.*) This argument is unavailing.

The determination of obviousness must consider, *inter alia*, whether a person of ordinary skill in the art would have been motivated to combine the prior art to achieve the claimed invention and whether there would have been a reasonable expectation of success in doing so. *Brown & Williamson Tobacco Corp. v. Philip Morris, Inc.*, 229 F.3d 1120, 1124 (Fed. Cir. 2000).

Medichem S.A. v. Rolabo S.L., 77 USPQ2d 1865, 1869 (Fed. Cir. 2006). Where the teachings of two or more prior art references conflict, the Examiner must weigh the power of each reference to suggest solutions to one of ordinary skill in the art, considering the degree to which one reference might accurately discredit another. *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991). If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984.) Furthermore, our reviewing court has held that "[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). *See also Para-Ordnance Mfg. v. SGS Importers Int'l,* 73 F.3d 1085, 1090 (Fed. Cir. 1995).

In this case, McCarthy's teaching of a table walk device as being a part of an MMU in no way discourages or precludes the MMU from being externally located from the table walk device. One of ordinary skill in the art would simply view McCarthy's teaching as a mere alternative for arranging the cited devices. Similarly, the ordinarily skilled artisan would view Arimilli's anticipatory teaching of externally locating the table walk device from the MMU as another alternative for arranging the devices. It therefore follows that Appellant has not shown that the Examiner erred in concluding that the combination of Arimilli and McCarthy renders claims 15, 16, and 18 unpatentable.

Claims 19, 21, and 22

Appellant argues that Zolnowsky does not cure the deficiencies of Arimilli as it pertains to independent claim 14 from which claims 19, 21, and 22 depend. (App. Br. 15.) As detailed in our discussion of claim 14, we found no such deficiencies in Arimilli for Zolnowsky to remedy. Further, Appellant argues that there is insufficient rationale to combine the cited references. We find that the cited combination teaches the claimed limitations, which are prior elements performing known functions to achieve a predictable result. It follows that Appellant has not shown that the Examiner erred in concluding that the combination of Arimilli and Zolnowsky renders claims 19, 21, and 22 unpatentable.

SUMMARY and DECISON

A. Appellant has not shown that the Examiner erred in concluding that:

1. Gaskins anticipates claims 23, 24, and 26 through 28 under 35 U.S.C. § 102(e).

2. Arimilli anticipates claims 14, 17, and 20 under 35 U.S.C. § 102(e).

3. The combination of Gaskins and McCarthy renders claim 25 unpatentable under 35 U.S.C. § 103(a).

4. The combination of Arimilli and McCarthy renders claims 15, 16, and 18 unpatentable under 35 U.S.C. § 103(a).

5. The combination of Arimilli and Zolnowski renders claims 19, 21, and 22 unpatentable under 35 U.S.C. § 103(a).

Therefore we affirm these rejections.

B. Appellant has shown that the Examiner erred in concluding that:

1. The combination of McCarthy and Roth renders claims 14 through 18, and 20 unpatentable under 35 U.S.C. § 103(a).

2. The combination of McCarthy, Roth, and Zolnowski renders claims 19, 21, and 22 unpatentable under 35 U.S.C. § 103(a).

Therefore we reverse these rejections.

C. Because we affirm at least one rejection for each claim on appeal, the decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

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